

HIGH-EFFICIENCY BROADBAND MONOLITHIC PSEUDOMORPHIC HEMT AMPLIFIERS AT Ka-BAND*

Hua Quen Tserng, Paul Saunier, and Yung-Chung Kao

Central Research Laboratories
Texas Instruments Incorporated
P. O. Box 655936, MS 134
Dallas, Texas 75265

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ABSTRACT

High-efficiency broadband (up to 7 GHz) monolithic Ka-band amplifiers using doped channel power pseudomorphic HEMTs have been demonstrated. Amplifiers with output powers as high as 500 mW and power-added-efficiencies as high as 40% were demonstrated.

INTRODUCTION

High-efficiency, compact solid-state amplifiers are needed for implementation in active aperture phased array antennas for applications in radars, communications, and EW systems. Advances in III-V compound three-terminal device technology have allowed the implementation of monolithic circuit technology for amplifier applications at millimeter-wave frequencies [1-6]. This paper reports the latest advances in using these heterostructure transistors in highly efficient broadband monolithic amplifiers at Ka-band frequencies. For comparison, Table 1 lists the performance of this work as well as other MMIC amplifiers reported at millimeter-wave frequencies [7-20]. As is shown, this work has advanced the state-of-the-art in Ka-band monolithic power amplifier technology in terms of broadband power and efficiency.

AMPLIFIER DESIGN

Pseudomorphic doped channel HEMTs with parallel gate fingers (0.25 μm gate length) and air bridge source interconnects were used in the MMIC amplifier design. FETs with gate width of 100 μm , 200 μm , and 400 μm were used in the designs of the reported amplifiers. The MBE grown structure consists of a doped InGaAs channel sandwiched between two wide bandgap donor layers (AlGaAs and GaAs). This InGaAs layer is 100 \AA thick, and

is doped $2 \times 10^{18} \text{ cm}^{-3}$. Both wide bandgap layers are also doped $2 \times 10^{18} \text{ cm}^{-3}$. The indium concentration is 20% to maximize the channel current. This structure offers several advantages for high-frequency operation: high current density (electrons are provided both by the doped channel layer and by the two AlGaAs/InGaAs and GaAs/InGaAs heterojunctions), good electron confinement, and high saturated electron velocity. This device structure has been used in high-efficiency, narrow-band MMIC amplifiers at Ka-band frequencies [10-13].

The amplifier design was based on small-signal device models with modified load-line for optimum large-signal performance. Devices of various sizes were included in the mask set for on-wafer rf probing for device modeling (S-parameters measurements) and diagnostic purposes. Discrete devices with gatewidths as large as 400 μm were included. Figures 1 and 2 shows, respectively, the measured and modeled S-parameters of 200 μm and 400 μm gatewidth devices over the 2 to 40 GHz frequency range. The agreement between the modeled and measured S-parameters is excellent. These devices were biased at a drain voltage of 4 V with drain current at 20% Id_{ss} .

Two types of cascaded two-stage amplifiers were designed. Simplified circuit schematic diagrams are shown in Figures 3 and 4. Figure 3 shows the amplifier with 100 μm and 200 μm devices. The resistors in the input matching circuit are used to "de-Q" the input for broadband matching. Figure 4 shows the two-stage amplifier with 400 μm and 800 μm gatewidth FETs. The second stage of this amplifier uses two 400 μm unit cells to minimize the gain degradation due to size effects. Both amplifiers use integrated bias networks to simplify the biasing requirements. The GaAs substrate thickness is 4 mils (0.1 mm). Photographs of the two amplifiers are shown in Figures 5 and 6. The chip dimensions are indicated in the figure captions.

AMPLIFIER PERFORMANCE

The two-stage (100 μm /200 μm gate width) amplifiers (Fig.5) had achieved an output power of 120 mW with at least 10-dB gain and up to 29% power-added efficiency over the 27 to 34 GHz band. Figure 7 shows the performance of one of these amplifiers. The best amplifier has achieved a peak power-added efficiency of 40.3% with 141 mW output and 11-dB gain at 31 GHz (Figure 8). The high-power two-stage amplifier (400 μm /800 μm gatewidth), shown in Figure 6, has achieved an output power of 500 mW with 8.5 dB gain and 32.3% power-added efficiency at 30 GHz (Figure 9). At a reduced output power of 350 mW, the power-added efficiency was a record 36%. These high-efficiency amplifiers were biased at approximately 20% of Id_{ss} under small-signal conditions. The drain current increases with increasing RF drive, indicating a near Class-B operation of the amplifiers.

CONCLUSION

Broadband (up to 7 GHz bandwidth) high-efficiency monolithic Ka-band amplifiers using doped channel power pseudomorphic HEMTs have been demonstrated. Amplifiers with output powers as high as 500 mW and power-added-efficiencies as high as 40% were demonstrated. These amplifiers will allow the development of efficient, millimeter-wave systems requiring the integration of a large number of compact, high-efficiency MMIC amplifiers with reduced prime power and cooling requirements.

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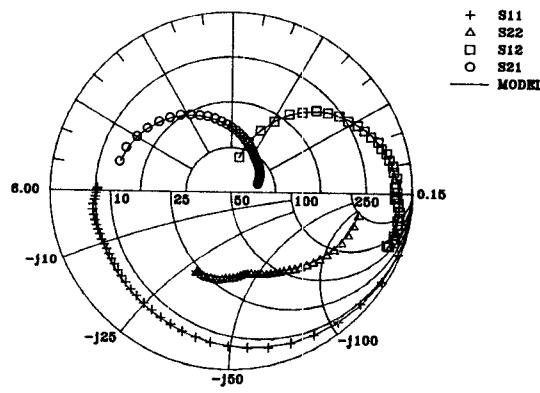
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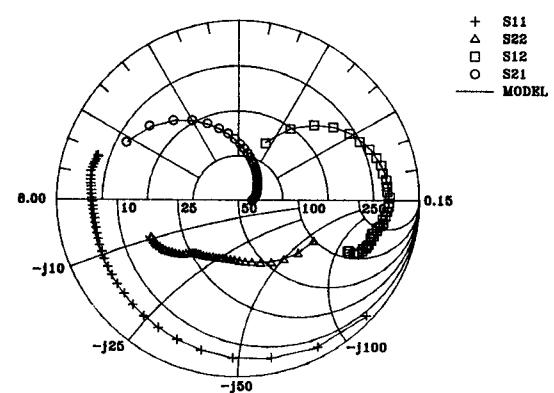
Table 1. Performance of Millimeter-Wave MMIC Amplifiers

Frequency (GHz)	Power (mW)	Gain (dB)	Efficiency (%)	B.W. (1-dB) (GHz)	# of Stages	Reference
28	480	4.3	11.2	1	1	7
28	1100	4.0	10.8	<1	1	8
28	560	7.2	15.0	1	2	9
29	450	16	25.0	2	3	11
31	190	23	30.2	1	3	10
31	720	4.2	24.0	3	1	11
31.5	54	4.8	34.0	<1	1	12
32	63	6.5	40.0	<1	1	13
32	72	13	31.3	<1	2	13
34	170	5	23.0	<1	1	14
34	112	16	21.6	1	3	15
41	140	4	15.7	1	1	16
42.5	180	4.6	14.0	2.5	1	17
58.5	95	4.5	11.0	3.5	1	18
36.0	220	20	21.5	4	3	19
44.0	250	8	11.0	3	3	20
30.0	126	10.5	27.8	7	2	This Work
31.0	141	11.0	40.3	4	2	This Work
30.0	500	8.5	32.3	6	2	This Work



2-40 GHz($V_g = -0.76V$, $V_d = 4V$, $I_d = 12.6$ mA)

Fig. 1. Modeled and measured S-parameters of a $200\ \mu\text{m}$ gatewidth HEMT.



2-40 GHz($V_g = -0.73V$, $V_d = 4V$, $I_d = 23.1$ mA)

Fig. 2. Modeled and measured S-parameters of a $400\ \mu\text{m}$ gatewidth HEMT

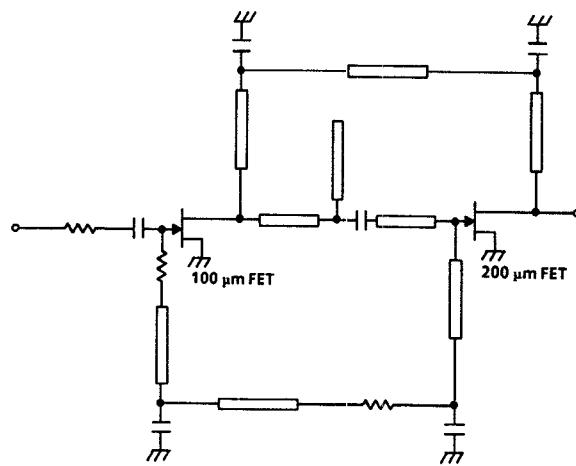


Fig. 3. Circuit diagram of a $100\ \mu\text{m}/200\ \mu\text{m}$ two-stage amplifier

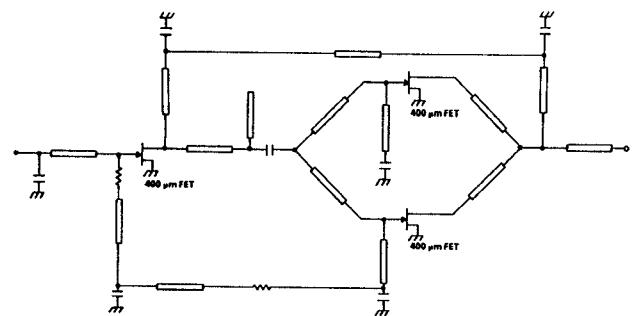


Fig. 4. Circuit diagram of a $400\ \mu\text{m}/800\ \mu\text{m}$ two-stage amplifier

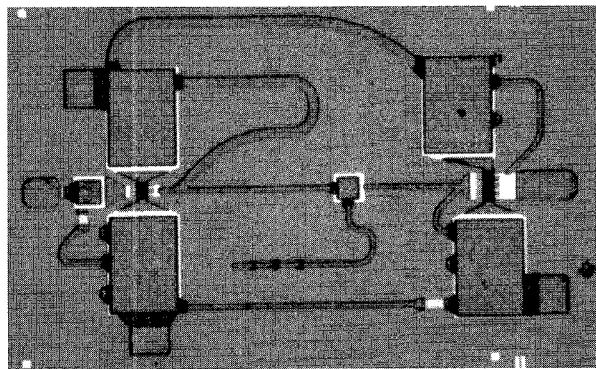


Fig. 5. Two-stage 100 μm /200 μm amplifier
(Chip size: 1.6 mm x 0.8 mm)

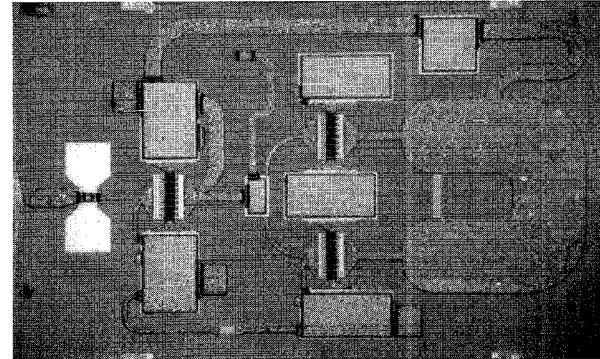


Fig. 6. Two-stage 400 μm /800 μm amplifier
(Chip size: 2.0 mm x 1.25 mm)

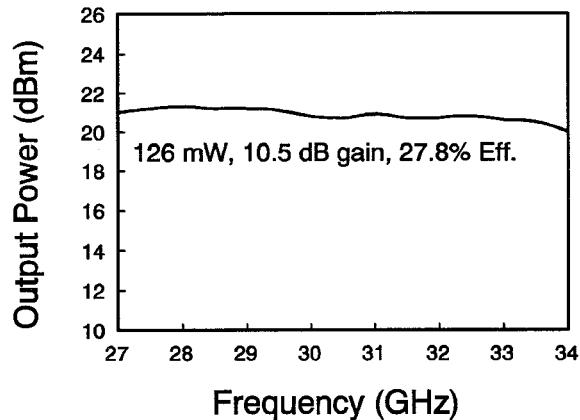


Fig. 7. Broadband performance of two-stage 100 μm /200 μm amplifier.

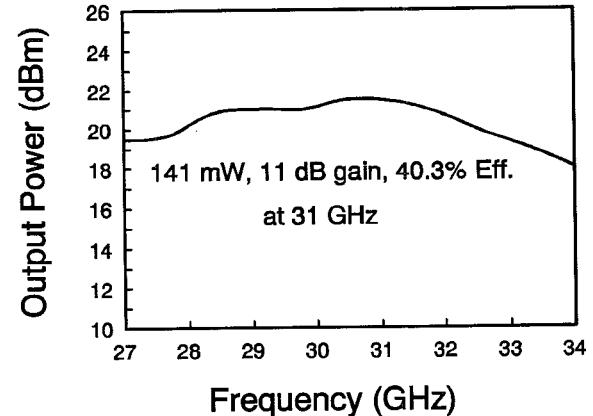


Fig. 8. High-efficiency performance of two-stage 100 μm /200 μm amplifier

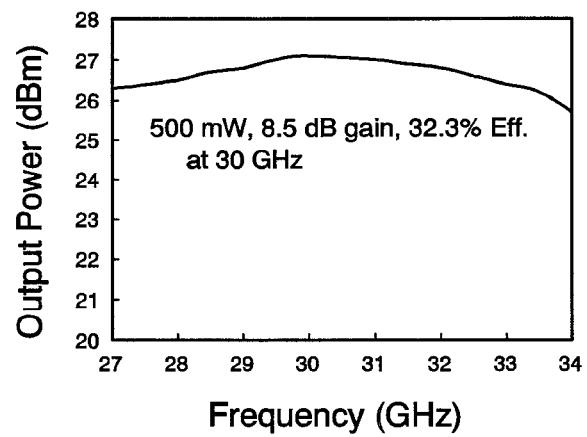


Fig. 9. Performance of two-stage 400 μm /800 μm amplifier.